IN THE CLAIMS

Amend the claims as follows.

1-5. (Cancelled)

6. (Previously Presented) A circuit, comprising:

a plurality of sampling-amplified-offset devices configured to sample, amplify, and compensate levels of an R charge signal, a G charge signal, and a B charge signal, respectively, and obtain an R analog signal, a G analog signal, and a B analog signal;

a gain adder configured to multiply at least one of the R, G, or B analog signals by a corresponding weighted value, wherein the gain adder is further configured to add at least a subset of the analog signals that are multiplied by the weighted values to obtain an addition analog signal; and

a multiplexer configured to select at least one of the R analog signal, the G analog signal, the B analog signal, or the addition analog signal as an output signal;

wherein at least one of the sampling-amplified-offset devices includes:

a sampler configured to obtain a plurality of samples of at least one of the R, G, or B charge signals and to determine a luminance based, at least in part, on a difference between at least two of the samples;

a programmable gain amplifier configured to obtain an amplified luminance according to a gain value; and

an offset device configured to compensate at least one of the R, G, or B analog signals, respectively, based, at least in part, on the obtained amplified luminance.

7. (Previously Presented) A circuit, comprising:

a plurality of sampling-amplified-offset devices configured to sample, amplify, and compensate levels of an R charge signal, a G charge signal, and a B charge signal, respectively, and obtain an R analog signal, a G analog signal, and a B analog signal;

a gain adder configured to multiply at least one of the R, G, or B analog signals by a corresponding weighted value, wherein the gain adder is further configured to add at least a subset of the analog signals that are multiplied by the weighted values to obtain an addition analog signal; and

a multiplexer configured to select at least one of the R analog signal, the G analog signal, the B analog signal, or the addition analog signal as an output signal;

wherein at least one of the sampling-amplified-offset devices includes:

a sampler configured to obtain a plurality of samples of at least one of the R, G, or B charge signals and to obtain a luminance;

an offset device configured to compensate a level of the luminance to obtain a compensated luminance; and

a programmable gain amplifier configured to adjust a gain value to amplify the compensated luminance and to obtain at least one of the R, G, or B analog signals.

8. (Currently Amended) The circuit of claim 6, wherein the gain adder comprises:

a plurality of gain amplifiers configured to multiply at least one of the R analog signal, the G analog signal, or the B analog signal by the corresponding weighted ~~gains~~ values to obtain a plurality of weighted analog signals; and

an adder configured to add the weighted analog signals to obtain the addition analog signal.

9. (Currently Amended) The circuit of claim 6, wherein the multiplexer is further configured to select at least one of the R, G, or B analog signals and output [[a]] the selected one to an analog-digital converter.

10. (Cancelled)

11. (Previously Presented) A circuit, comprising:

a plurality of sampling-amplified-offset devices configured to sample, amplify, and compensate levels of an R charge signal, a G charge signal, and a B charge signal, respectively, and obtain an R analog signal, a G analog signal, and a B analog signal;

a plurality of gain adders configured to multiply the R, G, and B analog signals by different weighted values to obtain a plurality of results, wherein the plurality of gain adders are further configured to add at least a subset of the results into an addition analog signal; and

a multiplexer configured to select the R analog signal, the G analog signal, the B analog signal, or the addition analog signal as an output;

wherein at least one of the sampling-amplified-offset devices includes:

a sampler configured to perform sampling at least twice on the R, G, or B charge signals and to perform a subtraction operation on sampling results to obtain a luminance;

a programmable gain amplifier configured to adjust a gain value to amplify the luminance and to obtain an amplified luminance according to the gain value; and

an offset device configured to compensate the amplified luminance to obtain the R, G, or B analog signal.

12. (Previously Presented) A circuit, comprising:

a plurality of sampling-amplified-offset devices configured to sample, amplify, and compensate levels of an R charge signal, a G charge signal, and a B charge signal, respectively, and obtain an R analog signal, a G analog signal, and a B analog signal;

a plurality of gain adders configured to multiply the R, G, and B analog signals by different weighted values to obtain a plurality of results, wherein the plurality of gain adders are further configured to add at least a subset of the results into an addition analog signal; and

a multiplexer configured to select the R analog signal, the G analog signal, the B analog signal, or the addition analog signal as an output;

wherein at least one of the sampling-amplified-offset devices includes:

a sampler configured to perform sampling at least twice on the R, G, or B charge signal and to perform a subtraction operation on sampling results to obtain a luminance;

an offset device configured to compensate a level of the luminance to obtain a compensated luminance; and

a programmable gain amplifier configured to adjust a gain value to amplify the compensated luminance and to obtain the R, G, or B analog signal.

13. (Currently Amended) The circuit of claim 11, wherein at least one of the gain adders comprises:

a plurality of gain amplifiers configured to multiply the R analog signal, the G analog signal, and the B analog signal by the corresponding weighted ~~gains~~ values to obtain a plurality of weighted analog signals; and

an adder configured to add the weighted analog signals to obtain the addition analog signal.

14. (Currently Amended) The circuit of claim 11, wherein the multiplexer is further configured to select at least one of the R, G, or B analog signals and output [[a]] the selected one to an analog-digital converter to form a digital signal.

15-17. (Cancelled)

18. (Currently Amended) The circuit of claim 7, wherein the gain adder comprises:

a plurality of gain amplifiers configured to multiply at least one of the R analog signal, the G analog signal, or the B analog signal by the corresponding weighted ~~gains~~ values to obtain a plurality of weighted analog signals; and

an adder configured to add the weighted analog signals to obtain the addition analog signal.

19. (Currently Amended) The circuit of claim 7, wherein the multiplexer is further configured to select at least one of the R, G, or B analog signals and output [[a]] the selected one to an analog-digital converter.

20. (Currently Amended) The circuit of claim 12, wherein one or more of the gain adders comprises:

a plurality of gain amplifiers configured to multiply the R analog signal, the G analog signal, and the B analog signal by the corresponding weighted ~~gains~~ values to obtain a plurality of weighted analog signals; and

an adder configured to add the weighted analog signals to obtain the addition analog signal.

21. (Currently Amended) The circuit of claim 12, wherein the multiplexer is further configured to select at least one of the R, G, or B analog signals and output [[a]] the selected one to an analog-digital converter to form a digital signal.